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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/963,257	09/26/2001	Shigeo Kusunoki	7217/65460	8381

7590 03/29/2005

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EXAMINER	
CHANG, EDITH M	
ART UNIT	**PAPER NUMBER**
2637	

DATE MAILED: 03/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/963,257	KUSUNOKI, SHIGEO	
	Examiner	Art Unit	
	Edith M Chang	2637	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 September 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 September 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *20030109,20050128*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 2-6, 8-12, 14, 20 and 29-35 are objected to because of the following informalities:

Claims 2 & 8, line 6: "data for amplitude" is suggested changing to " the data for amplitude".

Claims 6, 12, 20 & 29, line 4: "+1 bit" is suggested changing to "digital +1 bit", "-1 bit" is suggested changing to "digital -1 bit"; and line 5: "the result" is suggested changing to "the comparison result".

Claim 14, line 5: "are" is suggested changing to "is".

Claim 30, line 9: "input envelope detection step" is suggested changing to "detecting an input envelope step"; line 10: "output envelope detection" is suggested changing to "detecting an output envelope"; line 12: "comparison" is suggested changing to "comparing"; line 16: "comparison result correction" is suggested changing to "correcting"; and line 19: "amplitude control signal generation" is suggested changing to "generating an amplitude control signal".

Claim 31, line 5: "input envelope detection" is suggested changing to "detection an input envelope"; and lines 7-8: "phase control signal generation" is suggested changing to "generating a phase control signal".

Claim 32, line 10: "calculation" is suggested changing to "calculating"; line 13: "comparison" is suggested changing to "comparing"; line 17: "comparison result correction" is suggested changing to "correcting".

Claim 33, line 6: "a phase control step of controlling" is suggested changing to "controlling"; line 8: "phase control signal generation" is suggested changing to "generating a phase control signal".

Claim 34, lines 10-11 & 18: "phase control signal generation" is suggested changing to "generating a phase control signal"; lines 16-17: "phase difference detection" is suggested changing to "detecting phase difference"; and line 19: "phase control" is suggested changing to "controlling the phase".

Claim 35, line 10: "comparison result correction" is suggested changing to "correcting"; and line 13: "amplitude control signal generation" is suggested changing to "generating an amplitude control signal".

Claims 3-5 & 9-11 are directly or indirectly dependent on the objected claims 2 and 8 respectively.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 13-14, 22 and 23-29 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim 13 inherits the limitations of claim 7 comprising comparison means, and the apparatus further comprises two comparison means. Hence beside the comparison means inherited from claim 7, the apparatus further comprises another two comparison means. The disclosure of the drawings does not teach three comparison means.

Claim 23 as disclosed in FIG.14, lines 15-18 recite the phase difference detection means (PH_Det 37) detecting a phase difference between the input envelope voltage detected by the first envelope detection means (1 DET1) and the output envelope voltage detected by the second envelope detection means (15 DET2) that is not taught in the drawing FIG.14.

In FIG.14 the phase difference detection means (PH_Det 37) detects a phase difference between input signal PA_in prior applied to DET1 and output signal PA_out prior applied to DET2.

Claims 14 and 22 are dependent on the rejected claim 13; claims 24-29 are dependent on the rejected claim 23.

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 6, 12, 20 and 29 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 6, 12, 20 & 29, line 5: "the result" does not clearly indicate which result, the comparison result, the result of latching, or others.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1-5, 15-19, 23-28, 30-31 and 34-35 are rejected under 35 U.S.C. 102(e) as being anticipated by Wessel et al. (US 6,275,685 B1).

Regarding **claims 1 & 30**, in FIGURE 4-6, Wessel et al. teaches an amplifier arrangement and its method (FIGURE 4) with the Gain and phase error detectors (60 FIGURE 4 detailed in FIGURE 5) and the Adaptive Predistorter (70 FIGURE 4 detailed in FIGURE 6) to compensate the distortion generated in the power amplifier (PA 22 FIGURE 4). The amplifier arrangement comprises:

a first envelope detector (610 FIGURE 5, column 7 lines 16-27) to provide the voltage of the input signal (36 FIGURE 4 & 6);

a second envelop detector (612 FIGURE 5, column 7 lines 17-19) to provide the voltage of the output signal of the PA (50 FIGURE 4 as 54 feedback signal FIGURE 5);

a differential amplifier (as a comparator, 616 FIGURE 5, column 7 lines 20-23) to compare the signal voltages from the input and output of the PA (42 & 54 FIGURE 4);

a multiplier (754 for gain FIGURE 6), an adder (756 for gain FIGURE 6) and a buffer (758 FIGURE 6), as the comparison result correction means, to provide an improved estimate of the gain correction factor (the delta of the gain, column 9 lines 17-25) for the correction;

a RAM (740 for gain FIGURE 6), DAC (743 for gain FIGURE 6) and filter (744 for gain FIGURE 6 as the amplitude control signal generation means) to provide the Gain correction signal (92 FIGURE 6), as the amplitude control signal based on the result from the buffer;

an amplitude modulator (16 FIGURE 4, column 6 lines 37-39, as the amplitude control means) receives the Gain correction signal to control the gain of the input signal.

Regarding **claims 2-3 & 16-17**, in FIGURE 6, Wessel et al. teaches the Gain correction RAM 764 (as the amplitude correction data output means) outputting and updating data for the Gain correction signal 92 based on the input signal 36 and the correction output from the buffer 758 respectively (column 9 lines 15-25), and the RAM is a writable storage medium (764 FIGURE 6, column 8 lines 42-44).

Regarding **claims 4-5 & 18-19**, in FIGURE 6, Wessel et al. teaches the RAM 740 comprising two writable media, wherein the content of one medium of the RAM is read to Data bus to FIFO 736 in the phase one of the clock as the reading phase (column 8 lines 17-25 & 27-30) and the content of the 3-state buffer 758 is written to RAM 740 in the phase two of the clock (column 8 lines 42-44 & 49-52) separately from the content read in on phase one. Hence the RAM comprises two writable media, one for reading and one for writing alternatively.

Regarding **claims 15 & 31**, Wessel et al. teaches

a RAM (710 FIGURE 6, as the phase control signal generation means) to provide the Phase correction signal (94 FIGURE 6, as a phase control signal) for controlling the phase of the input signal (36 FIGURE 6); and

a phase modulator (18 FIGURE 4, as the phase control means) to control the phase of the input signal.

Regarding **claims 23 & 34**, in FIGURE 4-6, Wessel et al. teaches an amplifier arrangement and its method (FIGURE 4) with the Gain and phase error detectors (60 FIGURE 4 detailed in FIGURE 5) and the Adaptive Predistorter (70 FIGURE 4 detailed in FIGURE 6) to compensate the distortion generated in the power amplifier (PA 22 FIGURE 4). The amplifier arrangement comprises:

a first envelope detector (34 FIGURE 4, column 6 lines 41-44) to provide the voltage of the input signal (36 FIGURE 4 & 6);

a RAM (710 FIGURE 6, as the phase control signal generation means) to provide the Phase correction signal (94 FIGURE 6, as a phase control signal) for controlling the phase of the input signal (36 FIGURE 6);

a phase modulator (18 FIGURE 4, as the phase control means) to control the phase of the input signal;

a second envelop detector (612 FIGURE 5, column 7 lines 17-19) to provide the voltage of the output signal of the PA (50 FIGURE 4 as 54 feedback signal FIGURE 5);

a Phase comparator (630 FIGURE 5, as the phase difference detection means) to provide a Phase error signal (84 FIGURE 5, as the phase difference) between the input signal (42 FIGURE 5) and the output signal (54 FIGURE 5); and

an adder (726 FIGURE 6) adding the Phase error signal 84 and the output from the RAM 710 (the output of FIFO 716 FIGURE 6) to the Phase correction signal (94 FIGURE 6).

Regarding **claims 24 & 35**, Wessel et al. teaches

a differential amplifier (as a comparator, 616 FIGURE 5, column 7 lines 20-23) to compare the signal voltages from the input and output of the PA (42 & 54 FIGURE 4);

a multiplier (754 for gain FIGURE 6), an adder (756 for gain FIGURE 6) and a buffer (758 FIGURE 6), as the comparison result correction means, to provide an improved estimate of the gain correction factor (the delta of the gain, column 9 lines 17-25) for the correction.

a RAM (740 for gain FIGURE 6), DAC (743 for gain FIGURE 6) and filter (744 for gain FIGURE 6 as the amplitude control signal generation means) to provide the Gain correction signal (92 FIGURE 6, as the amplitude control signal) based on the result from the buffer;

an amplitude modulator (16 FIGURE 4, column 6 lines 37-39, as the amplitude control means) receives the Gain correction signal to control the gain of the input signal.

Regarding **claims 25 & 26**, in FIGURE 6, Wessel et al. teaches the Gain correction RAM 764 (as the amplitude correction data output means) outputting and updating data for the Gain correction signal 92 based on the input signal 36 and the correction output from the buffer 758 respectively (column 9 lines 15-25), and the RAM is a writable storage medium (764 FIGURE 6, column 8 lines 42-44).

Regarding **claims 27 & 28**, in FIGURE 6, Wessel et al. teaches the RAM 740 comprising two writable media, wherein the content of one medium of the RAM is read to Data bus to FIFO 736 in the phase one of the clock as the reading phase (column 8 lines 17-25 & 27-30) and the content of the 3-state buffer 758 is written to RAM 740 in the phase two of the clock (column 8 lines 42-44 & 49-52) separately from the content read in on phase one. Hence the RAM comprises two writable media, one for reading and one for writing alternatively.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 7-11, 13-14, 21-22 and 32-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wessel et al. (US 6,275,685 B1) in view of Eggleston et al. (US 4,987,378).

Regarding **claims 7, 13-14 & 32**, in FIGURE 4-6, Wessel et al. teaches an amplifier arrangement (FIGURE 4) with the Gain and phase error detectors (60 FIGURE 4 detailed in FIGURE 5) and the Adaptive Predistorter (70 FIGURE 4 detailed in FIGURE 6) to compensate the distortion generated in the power amplifier (PA 22 FIGURE 4). The amplifier arrangement comprises:

a first envelope detector (610 FIGURE 5, column 7 lines 16-27) to provide the voltage of the input signal (36 FIGURE 4 & 6);

a second envelop detector (612 FIGURE 5, column 7 lines 17-19) to provide the voltage of the output signal of the PA (50 FIGURE 4 as 54 feedback signal FIGURE 5);

a differential amplifier (as the calculation means and the comparator, 616 FIGURE 5, column 7 lines 20-23) to compare the signal voltages from the input and output of the PA (42 & 54 FIGURE 4);

a multiplier (754 for gain FIGURE 6), an adder (756 for gain FIGURE 6) and a buffer (758 FIGURE 6), as the comparison result correction means, to provide an improved estimate of the gain correction factor (the delta of the gain, column 9 lines 17-25) for the correction;

a RAM (740 for gain FIGURE 6), DAC (743 for gain FIGURE 6) and filter (744 for gain FIGURE 6 as the amplitude control signal generation means) to provide the Gain correction signal (92 FIGURE 6, as the amplitude control signal) based on the result from the buffer;

an amplitude modulator (16 FIGURE 4, column 6 lines 37-39, as the amplitude control means) receives the Gain correction signal to control the gain of the input signal.

Wessel et al. does not specify the predetermined reference values in the comparison. However, in FIG.1, Washburn et al. teaches the noise control circuit (21, column 3 lines 19-25) and the compensation circuit (50, column 4 lines 21-32) for controlling the power amplifier 11. The noise control circuit 20, as shown in FIG.2 and FIG.4A, uses the window comparator technique with two comparators and two predetermined reference values (operational amplifiers with V_{R1} & V_{R2} of FIG.4A) compared with the difference of the RF signal from the RF source (13) and the output of the amplifier 11 (column 5 lines 5-13 & column 6 lines 16-24).

As Wessel et al.'s pre-distortion is such as to cancel the AM-AM and AM-PM distortion of the power amplifier (Abstract lines 12-14) and Washburn et al. teaches a RF amplifier control circuit provides noise opposed and operation compensated pre-distortion control (21 & 50 FIG.1, column 3 lines 23-25 & column 4 lines 13-20). Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to have the window comparator with two predetermined reference vales (FIG.4A '583) taught by Washburn et al. in Wessel et al's comparator in the Gain and phase error detector (60 FIGURE 4 '685) to reduce the amplitude modulation (AM, column 3 lines 60-64) and phase modulation (PM, column 4 lines 47-50) noise/distortion and to prevent the amplifier from being overdriven (column 1 lines 25-30).

Regarding **claims 8-9**, in FIGURE 6, Wessel et al. teaches the Gain correction RAM 764 (as the amplitude correction data output means) outputting and updating data for the Gain correction signal 92 based on the input signal 36 and the correction output from the buffer 758 respectively (column 9 lines 15-25), and the RAM is a writable storage medium (764 FIGURE 6, column 8 lines 42-44).

Regarding **claims 10-11**, in FIGURE 6, Wessel et al. teaches the RAM 740 comprising two writable media, wherein the content of one medium of the RAM is read to Data bus to FIFO 736 in the phase one of the clock as the reading phase (column 8 lines 17-25 & 27-30) and the content of the 3-state buffer 758 is written to RAM 740 in the phase two of the clock (column 8 lines 42-44 & 49-52) separately from the content read in on phase one. Hence the RAM comprises two writable media, one for reading and one for writing alternatively.

Regarding **claims 21-22 & 33**, Wessel et al. teaches

a RAM (710 FIGURE 6, as the phase control signal generation means) to provide the Phase correction signal (94 FIGURE 6, as a phase control signal) for controlling the phase of the input signal (36 FIGURE 6); and

a phase modulator (18 FIGURE 4, as the phase control means) to control the phase of the input signal.

Allowable Subject Matter

10. Claims 6, 12, 20 and 29 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

11. The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record fails to teach or suggest, alone or in a combination, among other things, at least a distortion compensation apparatus for compensating for a distortion component generated in a device and its method as a whole, the combination of elements and features, which includes latches the comparison result of the input signal to the device and the output feedback signal from the device, and corrects and outputs on e of a digital 1 bit and a digital –1 bit based on a latch value of the result.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Edith M Chang whose telephone number is 571-272-3041. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jayanti Patel can be reached on 571-272-2988. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Edith Chang
March 16, 2005

YOUNG T. TSE
PRIMARY EXAMINER